



UNITED STATES PATENT AND TRADEMARK OFFICE

8/6
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,105	11/14/2000	Hirokazu Honda	NEC 00USFP553	7050

7590 08/14/2002

Norman P. Soloway
HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C.
175 Canal Street
Manchester, NH 03101

EXAMINER

THAI, LUAN C

ART UNIT	PAPER NUMBER
	2827

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	09/712,105	HONDA, HIROKAZU
	Examiner Luan Thai	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 May 2002.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

4) Claim(s) 25-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 25-49 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4) Interview Summary (PTO-413) Paper No(s) _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

This Office action is responsive to the amendment filed May 15, 2002.

Claims **25-49** (newly added claims) are pending in this application.

Claims **1-24** have been canceled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims **32** and **43-46** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **32**, the limitations "said conductive bump and another conductive bump" have no antecedent basis and unclear as to whether those limitations imply the first conductive bumps or the second conductive bumps.

In claim **43**, the recitation of "said first stress buffering layer" has no antecedent basis.

Claims **44-46** are rejected since each includes the limitations of claim **43**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2827

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. **Claims 37, 39-40, 42-44 and 48**, insofar as in compliance with 35 USC 112, are (is) rejected under 35 U.S.C. 102(e) as being anticipated by Yamaji et al. (6,159,837).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 37, 39-40, 42-44 and 48, Yamaji et al disclose (see specifically figures 4-6) a semiconductor device, comprising: pads 2 formed on a semiconductor chip 1; conductive sections 4 connected to pads 2 via wiring patterns 4 provided on the chip; conductive columns 7 on surfaces of the conductive sections 4, having a height of 25 to 100 μ m and being covered other than at their top surfaces with an polyimide stress buffering layer 5, wherein wiring patterns 4 extend to adjust a pitch between conductive columns 7; conductive bumps 8 on exposed surfaces of the conductive columns 7; a passivation layer 3 underlying the stress buffering layer and covering the chip other than the pads; a second insulating film 5a, figure 6, (note the insulating layer 9 in figure 4 can also be considered as the second insulating film) formed between the passivation film and the stress buffering layer.

4. **Claims 25 and 28-31** are (is) rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (4,751,349).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 25 and 28-31, Kim et al disclose (see specifically figure

1) a semiconductor device, comprising: a plurality of pads formed on a semiconductor chip 34 for solder balls 32 electrically connected to; conductive sections 20 connected to pads 2 via wiring patterns 31 (formed of copper) and solder balls 32 provided on the chip; first conductive bumps 27 on surfaces of the conductive sections 20 and covered other than at their top surfaces with first electrically insulating stress buffering layer 37 of polyimide; a second conductive bumps 26 on exposed top surfaces of the first conductive bumps 27, and covered other than at their top surfaces with a second electrically insulating stress buffering layer 36.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claim 38** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Farrar (6,077,792 of record) and Goto et al. (6,214,923 of record), separately.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 38, Yamaji et al. disclose all the limitations of the claimed invention as detailed above except for teaching the stress-buffering layer having an elastic modulus in a range of 0.01 to 8 Gpa.

A stress-buffering layer made of polyimide and having an elastic modulus in a range of 0.01 to 8 Gpa, however, is conventional in the art, as taught by both Farrar (Col. 5, lines 44+) and Goto et al. (Col. 24, lines 24+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the polyimide stress buffering layer having an elastic modulus in the claimed range in Yamaji et al.'s device since such the claimed polyimide layer is conventionally used in the art.

7. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Yamamoto (5,925,931 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 41, Yamaji et al disclose all the limitations of the claimed invention as detailed above except for teaching the wiring pattern being made of copper.

Copper is a well known material in semiconductor art for making wiring pattern, as taught by Yamamoto (Col. 5, lines 17+). It would have been obvious

Art Unit: 2827

to one of ordinary skill in the art at the time the invention was made to use copper for forming the wiring pattern in Yamaji et al's device since copper is a well-known material in the semiconductor art for forming wiring pattern.

8. Claim 45, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Kasahara et al. (5,790,362 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 45, Yamaji et al. disclose all the limitations of the claimed invention as detailed above except for teaching the second insulating film having a pyrolysis temperature of 200 degree C or more.

Yamaji et al. do teach the second insulating film 5a being made of polyimide, and it is apparent that a polyimide film, which has a pyrolysis temperature of 200 degree C or more, is conventional in the art, as disclosed by Kasahara et al. (Col. 9, lines 7+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use polyimide film having a pyrolysis temperature as claimed since such material is conventionally used in the semiconductor art.

9. Claim 46, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Chakravorty (6,181,569 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 46, Yamaji et al. disclose all the limitations of the claimed invention as detailed above except for teaching the second insulating film being formed of a photosensitive material. Yamaji et al do disclose the second insulating film being a polyimide film.

Chakravorty while related to a similar Chip-Size-Package design teach an insulating film formed on a semiconductor chip is made of a photosensitive material, such as the photosensitive polyimide (Col. 8, lines 18+). Thus, a photosensitive polyimide film is conventional in semiconductor art for forming an insulating layer on the chip surface. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use photosensitive polyimide to form the second insulating film in the device of Yamaji et al. since such material is conventionally used in the semiconductor art.

10. Claim 47, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Sawai et al (5,554,887 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 47, Yamaji et al discloses all the limitations of the claimed invention as detailed above except for teaching the wiring pattern being made of copper.

Sawai et al while related to a similar chip-size-package design teach (see specifically figures 8 and 11-12) conductive columns 4 formed on a semiconductor chip 1 are made of copper (Col. 14, lines 15+). Thus, conductive columns being made of copper are conventional in semiconductor art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply conductive columns of copper to the device of Yamaji et al, since copper is a well-known material in the art for making conductive columns.

11. Claim 49, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al. (6,159,837) in view of Sawai et al (5,554,887).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 49, Yamaji et al discloses all the limitations of the claimed invention as detailed above except for explicitly teaching the conductive columns being circular in cross section.

Sawai et al while related to a similar chip-size-package design teach (see specifically figures 8 and 11-12) conductive columns 4 formed on a semiconductor chip 1 are circular in cross section. Thus, conductive columns

being circular in cross section are conventional in semiconductor art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply conductive columns being circular in cross section to the device of Yamaji et al, since such conductive columns structure are conventional in the art.

12. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (4,751,349) in view of Farrar (6,077,792 of record) and Goto et al. (6,214,923 of record), separately.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 38, Kim et al. discloses all the limitations of the claimed invention as detailed above except for teaching the stress buffering layer having an elastic modulus in a range of 0.01 to 8 Gpa.

A stress-buffering layer made of polyimide and having an elastic modulus in a range of 0.01 to 8 Gpa, however, is conventional in the art, as taught by both Farrar (Col. 5, lines 44+) and Goto et al. (Col. 24, lines 24+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the polyimide stress-buffering layer having an elastic modulus in the claimed range since such polyimide layer is conventionally used in the art.

13. Claim 32, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (4,751,349) in view of Miles et al (5,535,101).

Art Unit: 2827

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 32, Kim et al. discloses all the limitations of the claimed invention as detailed above except for the wiring pattern extending to adjust a pitch between the conductive bump and another conductive bump.

Miles et al teach while related to a similar semiconductor package design teach the wiring pattern 20 extending to adjust a pitch between the conductive bump 22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim et al's wiring pattern 31 by extending this wiring pattern to adjust a pitch between the conductive bumps 20, as taught by Miles et al.

14. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (4,751,349) in view of Yamamoto (5,925,931 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 33-34, Kim et al. discloses all the limitations of the claimed invention as detailed above except for detailing the active surface structure of the chip 34 that includes a passivation film covering the active surface of the chip other than the electrode pads formed on the chip and an insulating film formed on the passivation film.

Yamamoto while related to a semiconductor chip design teaches includes a passivation film 24 covering the active surface of the chip 22 other than the electrode

Art Unit: 2827

pads 23 formed on the chip and a polyimide insulating film 41 formed on the passivation film in order to protect the circuit formed on the active surface of the chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form chip 34 with the structure of a passivation film and a polyimide insulating film, as taught by Yamamoto, for the purpose of protecting the circuit formed on the active surface of the chip. Since the proposed semiconductor chip 34 of Kim et al and Yamamoto electrically connected to bumps 20 (via wiring pattern 31 and solder balls 32, see Kim et al's figure 1), the insulating film is obviously positioned between the passivation film and the first stress buffering layer 38.

15. **Claim 35**, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (4,751,349) in view of Yamamoto (5,925,931 of record) and further in view of Kasahara et al. (5,790,362 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 35, the proposed device package of Kim et al. and Yamamoto discloses all the limitations of the claimed invention as detailed above except for teaching the second insulating film (e.g., the polyimide insulating film) having a pyrolysis temperature of 200 degree C or more.

A polyimide film, which has a pyrolysis temperature of 200 degree C or more, however, is conventional in the art as disclosed by Kasahara et al. (Col. 9, lines 7+). It would have been obvious to one of ordinary skill in the art at the time

- Art Unit: 2827

the invention was made to use polyimide film having a pyrolysis temperature as claimed in the proposed device package of Kim et al. and Yamamoto since such material is conventionally used in the semiconductor art.

16. Claim 36, insofar as in compliance with 35 USC 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (4,751,349) in view of Yamamoto (5,925,931 of record) and further in view of Chakravorty (6,181,569 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 36, the proposed device package of Kim et al. and Yamamoto discloses all the limitations of the claimed invention as detailed above except for teaching the second polyimide insulating film being formed of a photosensitive material.

Chakravorty while related to a similar Chip-Size-Package design teach an insulating film formed on a semiconductor chip is made of a photosensitive material, such as the photosensitive polyimide (Col. 8, lines 18+). Thus, a photosensitive polyimide film is conventional in semiconductor art for forming an insulating layer on the chip surface. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use photosensitive polyimide to form the second insulating film in the proposed device package of Kim et al. and Yamamoto since such material is conventionally used in the semiconductor art.

• Art Unit: 2827

Conclusion

17. Applicant's arguments with respect to newly added claims **25-49** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the underlined portions of newly added claims 25-49 raise new issues that would require further consideration and/or search. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

Application/Control Number: 09/712,105

Page 14

Art Unit: 2827

308-7722 for regular communications and (703) 308-7724 for After Final
communications.

Any inquiry of a general nature or relating to the status of this application or
proceeding should be directed to the receptionist whose telephone number is (703) 308-
0956.

Luan Thai
August 9, 2002


Kunio
Primary Examiner